MoS_2 nanosheets based Electric Double Layer Transistor

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Abstract

With the advancement of the present research in the field of transistors, with the miniaturization of devices it has become a great challenge of achieving high carrier density and lower operational voltage in the conventional field effect transistors, where in the normal case we usually see low capacitance and dielectric breakdown of gate dielectrics. And hence, presently, the development of the electric double layer technology with high charge career accumulation at the channel/electrolyte interface has been successful to achieve this motto. And presently several other superior characteristics like- superconductivity, metal insulator transition and tunable thermoelectric behaviour have been observed both theoretically and experimentally.

Keywords: *Channel material, gate material, capacitance, field effect mobility, sub-threshold swing*

1. Introduction

Recently the Electric Double Layer technology has become a novel and attractive technology in the field of electronics because it can achieve higher carrier concentration compared with the conventional FET. The key characteristic in the EDLT is the formation of the electric bi-layer or double layer based on the electrolytes such as ionic liquids and polymer electrolytes such as ionic liquids and polymer electrolytes with mobile charges.

The EDL concept was generated from the research work on the super capacitors, and the operation of the electric double layer capacitors is different from that of the conventional capacitors. Fig.1 shows that an electrolyte (liquid or solid) with mobile cations and anions is filled between the two electrodes. There are several models regarding the formation of the electric double layers. The first one is obviously the Helmholtz model. When an electronic conductor is brought in close contact with a solid or liquid ionic conductor (i.e. the electrolyte), a common interface will appear between the two phases. It was Helmholtz's superiority to realize for the first time that when charged electrodes are immersed in the electrolyte solution, they will repel the co-ions and will attract the counter ions and at the same time two layers of opposite polarity will be formed at the interface between the electrode and the electrolyte. He showed in 1853 that this bi-layer is essentially a molecular dielectric and stores the charge electrostatically.

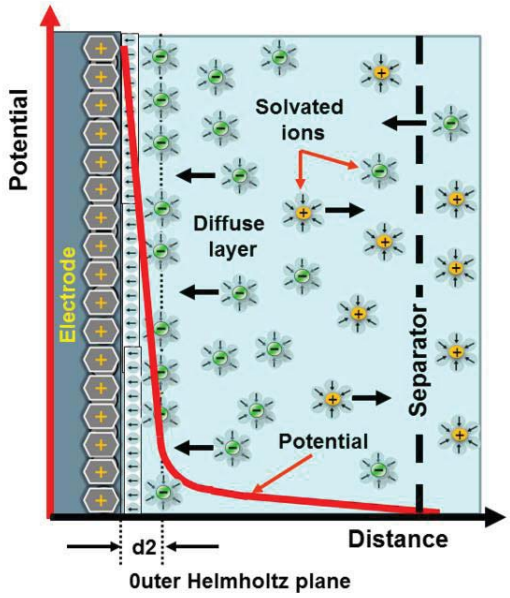

FIG.1: Simplified illustration of the potential development in the area and in the further course of a Helmholtz double layer

2. Electric Double Layers

As mentioned above, The EDLT concept was introduced from the research of the supercapacitors and the function of the electric double layer capacitors is different from that of the conventional capacitors. The below figure shows the operation mechanism of the EDLC. As shown in the figure we can see that the mobile cations and anions are filled between the electrodes and the electric double layer is formed at the interface of the channel/electrolyte interface. When voltage is applied externally, the cations and the anions move towards the surface of the electric double layer, which is known as the charging process. This double layer consists of the space charge from the electrode side and ion space charge from the electrolyte side. Here, the capacitance is proportional to the cross sectional area of the electric double layer and the operation is based on the absorption and desorption of the electric double layer.

In contrast, when the external voltage has been removed and load resistance is added, ions will move away and this is the discharge process. There are mainly three models which can describe the process of formation of the double layer- Helmholtz model, Gouy-Chapman model and Stern model. The Helmholtz model has been already explained in the introduction part. Here, we shall discuss about the development of the theory. They observed that the capacitance was not a constant quantity and it depends upon the applied potential and the ionic concentration. This model introduces a new concept of diffusion layer. In this model the charge distribution is actually a function of distance from the metallic surface which allows the Maxwell-Boltzmann statistics to be applied. Thus the electric potential decreases exponentially away from the surface of the fluid bulk. And thirdly, there comes the Stern model which is actually the modification of the Helmholtz model and the Gouy-Chapman model and this model is well fitted with the highly charged double

layers. The Stern layer accounts for the ion's finite size and consequently the ion's closest approach towards the electrode is of the order of ionic radius.

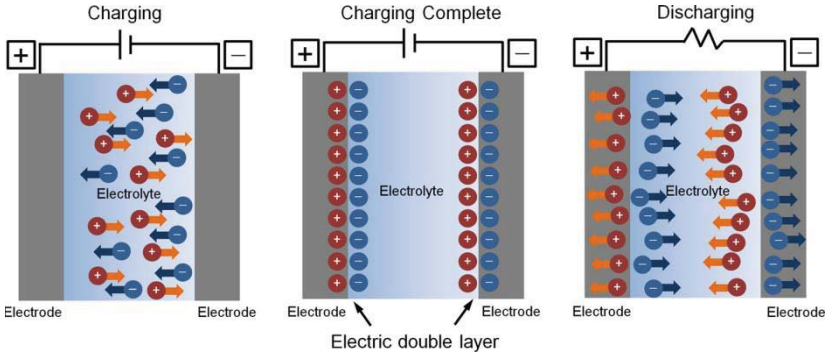

FIG.2: Charge and discharge of EDL capacitors. With permission from American Chemical Society.

2.1. Configurations of EDLTs

The EDLC concept tells us that the ultra-high capacitance is due to the formation of the electric double layer. If one electrode is substituted by a semiconductor and it is attached to the drain and source electrodes, the EDLC gets transformed to the Transistors. The gate becomes separated from the semiconductor by the electrolyte. EDL can be formed at the gate/electrolyte and semiconductor/electrolyte interface when a gate voltage is applied. Thus this transistor is called as the Electric Double Layer Transistor (EDLT).

2.1.1. Channel layer materials in EDLTs

There are mainly two types of materials which are used in the channel, i.e. metal oxide semiconductors and dichalcogenide semiconductors.

2.1.1.1. Metal oxide semiconductors

There are several types of oxide semiconductors, among which, one of the important is the Zinc oxide (ZnO) which has been applied in several fields like sensors, nano-generators, transistors etc. Yuan et al. has researched on the fact of fabricating transistors by using ZnO as the channel material and the ionic liquids as the gate material and they observed that, (i) inner Helmholtz layer can be created which can increase the capacitance and accumulate the charge carriers; (ii) surface polarity and surface atom recognition can be achieved by controlling the chemisorptions and physisorption of the H+ and the OH- ions on the polar ZnO surface; (iii) proton memory can be induced by the hydrogenation of the surface. On the other hand, they established a temperature-frequency mapping of EIS as the "phase diagram" to distinguish the electrostatic or electrochemical the charged EDL.

2.1.1.2. TMDs

The layered transition metal dichalcogenides (TMDs) are composed of the layered crystal structures with stacked planes, where the chalcogen and the metallic atoms are covalently bonded whereas the adjacent layers are bonded by the Vander wall's force of attraction.MoS_2 has usually two types of structures- 2H type and 3R type, where the 2H type structure is more stable than the 3R type structure, since the MX_2 with atomically flat surface can be easily made by means of cleavage. There are several other types of TMDs, like SnS_2. By using these, we have been able to get high capacitance, high on current, high on-off ratio, low operational voltage, low sub threshold swing etc. which were verified in several research works.

2.1.1.3. Organic channel layers

Organic semiconductors are usually regarded as a viable option for flexible electronics. Among organic compounds rubrene, pentacene, with outstanding charge carrier mobility and high on-off ratio are the chosen channel material. Frisbie et al. reported organic rubrene crystal based EDLT which was gated with the high capacitance ionic liquid. The maximum charge density of $3.5 \pm 1.2 \times 10^{13}$ cm^{-2} and maximum specific capacitance of 8.0±2.2 $\mu F/cm^2$ were achieved simultaneously at the gate voltage of -1V, while the mobility was low.

Liquid polymer electrolyte-gated rubrene single-crystal was investigated by Shimotani et al. They obtained larger field-effect mobility of 0.79 cm^2V^{-1}.They also used the four probe measurements from which they obtained the reversible peak in the transfer characteristics curve, which implies that the contact resistance increases with decrease in the drain current. Along with this pentacene, P(VPA-AA), poly (3-hexylthiopthene) can also be used for the same purpose.

Presently, carbon nanotubes, grapheme, perovskite materials are also used for the same purpose. The research is still in progress with the advancement of science and technology.

2.1.2. Electrolytes in EDLTs

For the gate-insulator the most important characteristic is the specific capacitance, implying that at a given gate voltage, the carriers can be induced in the semiconductor channel of the FETs. For long time in research work, SiO_2 is used having relatively low capacitance. However for the solid electrolytes, the capacitance is a very limited quantity because, their thickness cannot be reduced. Alternatively electrolytes are the suitable candidates because they can accumulate a large carrier density induced by the EDL at the electrolyte semiconductor interface. There are several types of electrolytes till now which are explained below.

2.1.2.1. Polymer electrolytes

These can be easily fabricated with good bendability and they are compatible with flexible substrates for electronic application in roll-to-roll technology. These types of electrolytes usually consist of different ions and polymer solvents. A typical example is obviously polyethylene oxide (PEO)/$LiClO_4$, where the Li^+ and ClO_4^- are dissolved in the polymer matrix and they can migrate under the application of the electric field. There is again another type of polymer electrolytes, i.e. pBTTT-C14 through which we can obtain high current densities, metallic conductivities etc. There are several research works regarding these electrolyte materials.

2.1.2.2. Polyelectrolytes

These usually consist of either positively or negatively charged ionizable groups. The difference between the polymer electrolyte and polyelectrolyte is that, in polymer electrolyte both the cations and anions can move, but in case of the polyelectrolyte only cations can move and anions are immobile due to the covalent bonding to the polymer backbone. And since the anions cannot move and penetrate the bulk semiconductor, it suppresses the electrochemical bulk doping. This superior property of polyeletrolytes enables the organic FETs to work entirely in the field-effect mode.

Among the polyelectrolytes, the typical representatives are PSSH and P(VPA-AA). PSSH and P3HT transistors exhibit fast responding (0.5ms), high current throughput and lower operational voltage (<1V). Not only that, but also faster switching speed (0.2ms) and clear pinch-off behaviour are observed.

2.1.2.3. Ionic liquids and gels

So by the research works, we have come to know that by using the polymer electrolytes gated OFETs, low switching speed has been obtained which limits the operational frequencies and also the response to the electric field and to overcome this problem, faster ion diffusivity is the most desired property. Thus the ionic liquids with high ion mobility and diffusivity have been studied. The first EDLT gated with the ionic liquids was first reported by Hebard and coworkers. They used InO_x as the channel material and AlO_x as the gate dielectrics. They reported that the gate-induced can be frozen below the glass transition temperature with the gate voltage which explores the fact of electric field tuning of the metal-insulator transitions in the transistors. Other several research works were reported in several times some reporting larger capacitance, some reporting larger field-effect mobility etc.

2.1.2.4. Inorganic solid-state electrolyte

With the progress in research work, it has been observed that with compared to the polymer electrolyte and ionic liquids, inorganic electrolytes show well chemical stability and comparable conductivity. Several studies have been done with the solid state insulators including SiO_2 and Al_2O_3, and it has been found

interestingly that solid state dielectrics with micro porous structures show greater conductivity. With relatively higher capacitance, inorganic non-metallic compounds like the micro porous SiO_2, Al_2O_3, zeolite, phosphosilicate glass, copolymer sodium alginate show the property of forming electric double layer, specially based on the property of proton conduction in nanofluid devices.

3. Device performance

To evaluate the device performance, several electrical parameters such as capacitance (C), field-effect mobility (μ_{FE}), on/off ratio, sub threshold swing (SS), transconductance (g_m) is mainly measured.

It is necessary to maximize the capacitance of the gate insulators for having (i) much higher output current at a given gate voltage, (ii) much lower power consumption, (iii) low threshold voltage.

$$C=\frac{\epsilon_0 KA}{t}$$

Mobility is defined as the average drift speed of carriers per unit electric field. It the FET has higher mobility; it implies more carriers passing through the channel per unit time, which is the most desirable property of small sized FETs. With higher mobility, higher screen luminescence and screen resolution can be achieved. Not only that, but also it helps in increasing the switching speed as well as decreasing the power consumption.

$$\mu_{FE}=\frac{Lg_m}{WCV_{DS}}$$

On/off ratio can be defined as the ration of the $I_{D,max}$ to $I_{D,min}$. The I_{on} depends upon the channel materials, device geometry like channel length, width, thickness, insulator capacitance and the gate voltage. I_{off} is related to the gate leakage and the resistivity of the channel layer.

$$\frac{I_{on}}{I_{off}}=\frac{I_{D,max}}{I_{D,min}}$$

Sub-threshold swing (SS) reflects the necessary V_G to increase the I_{DS} by an order of magnitude in the sub-threshold region, where $V_{GS}<V_{th}$.

$$SS=\left(\frac{d\log(I_{DS})}{dV_{GS}}|_{max}\right)^{-1}$$

For example, a typical SS of FETs is 80 mV/decade, which means that there is an 80 mV increase in V_G and leads to tenfold increase in the I_{DS}.

Transconductance can be defined as the increase in the drain current per unit increase in the gate-to-source voltage.

$$g_m=\frac{\partial I_D}{\partial V_{GS}}|V_{DS}=\text{constant}$$

4. Experimental

4.1. Materials and Apparatus

So in our experiment for the fabrication of the EDLT, we have used MoS_2 as the channel material. The ($PVA+H_2SO_4$) gel is used as the gate material. The apparatus which were needed in our experiment were- gold coated PET, ITO coated PET, copper wire, sonicating machine, cellulose film, vacuum pump.

4.2. Why MoS_2 as channel material

There are several types of materials those can be used as the channel material for the fabrication of the electric double layer transistor. But here we are using MoS_2 due to some its important properties- (i) MoS2 has layered structures. A plane of Mo atoms is sandwiched by two planes of sulphide ions. These three planes together form a monolayer of MoS_2. Bulk MoS_2 consists of such layers stacked one after another. These layers are kept together by weak Vander Waals force. It has an intrinsic layer gap of about 7 Angstrom; (ii) it has very good thermal stability and chemical stability; (iii) it can form highly efficient and dry lubricating films; (iv) it has large effective surface area; (v) 2-D MoS_2 has increased absorption capacity compared to the bulk material; (vi) very high melting point; (vii) relatively unreactive compound, does not react with dilute acid and oxygen.

4.3. Why ($PVA+H_2SO_4$) as gate material

There are several types of electrolyte materials which can be used as the gate material for the fabrication of the EDLT. Here we are using ($PVA+H_2SO_4$) as the gate material due to its several properties like- (i) Flexible devices can be fabricated; (ii) by using electrolyte, positive and negative carriers can be accumulated at the channel/electrolyte interface by applying the external electric field. Therefore, the EDL at the insulator/channel interface is formed and a new kind of transistor with much improved carrier mobility and density can be achieved.

4.4. Synthesis of MoS_2

We have used the hydrothermal method for the synthesis of MoS_2. Firstly, we have taken 0.25 gm of Na_2MoO_4, $2H_2O$ (sodium molybdate) and 0.5 gm of L-cysteine and have undergone the hydrothermal reaction inside the Teflon chamber at 220℃ for 30 hours. Then after natural cooling we have obtained the black coloured solution and finally washing and drying it at 60℃ for 12 hours we have obtained the black coloured powder of MoS_2. Here is the schematic diagram of this whole process:

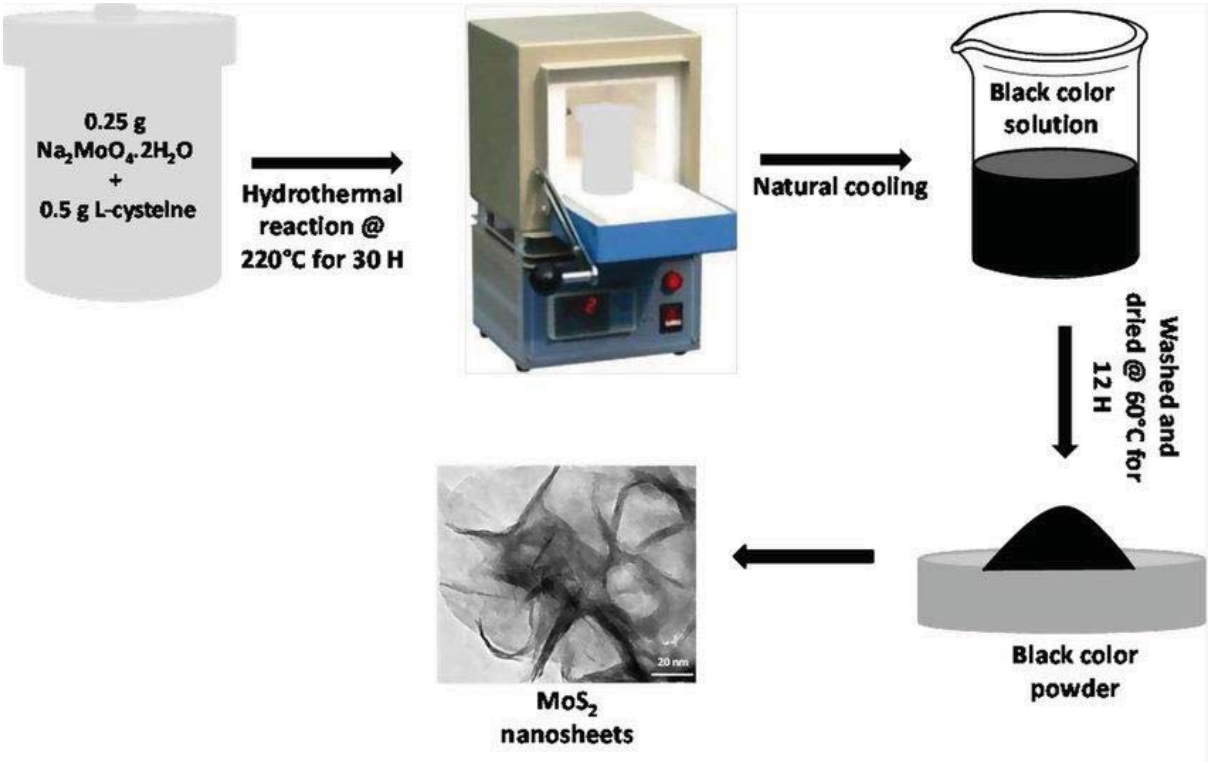

FIG. 3: Preparation of the MoS_2 in laboratory by Hydrothermal Process

4.5. Thin film of MoS_2

Firstly, the sample of MoS_2 is diluted with water to make the sample volume around 15 ml. Now place the cellulose membrane and switch on the pump after pouring few amounts of water on the membrane and it is kept for 10-15 minutes until it becomes dried. Now the pump is switched off. Next, the sample is poured on the membrane slowly and cautiously. Again the pump is switched on and lest for drying for 20-25 minutes. Now keeping the pump on, distilled water is poured cautiously on the membrane for washing and kept it for about 20-25 minutes. So in this way, the MoS_2 thin film is fabricated and is ready for further steps of the experiment.

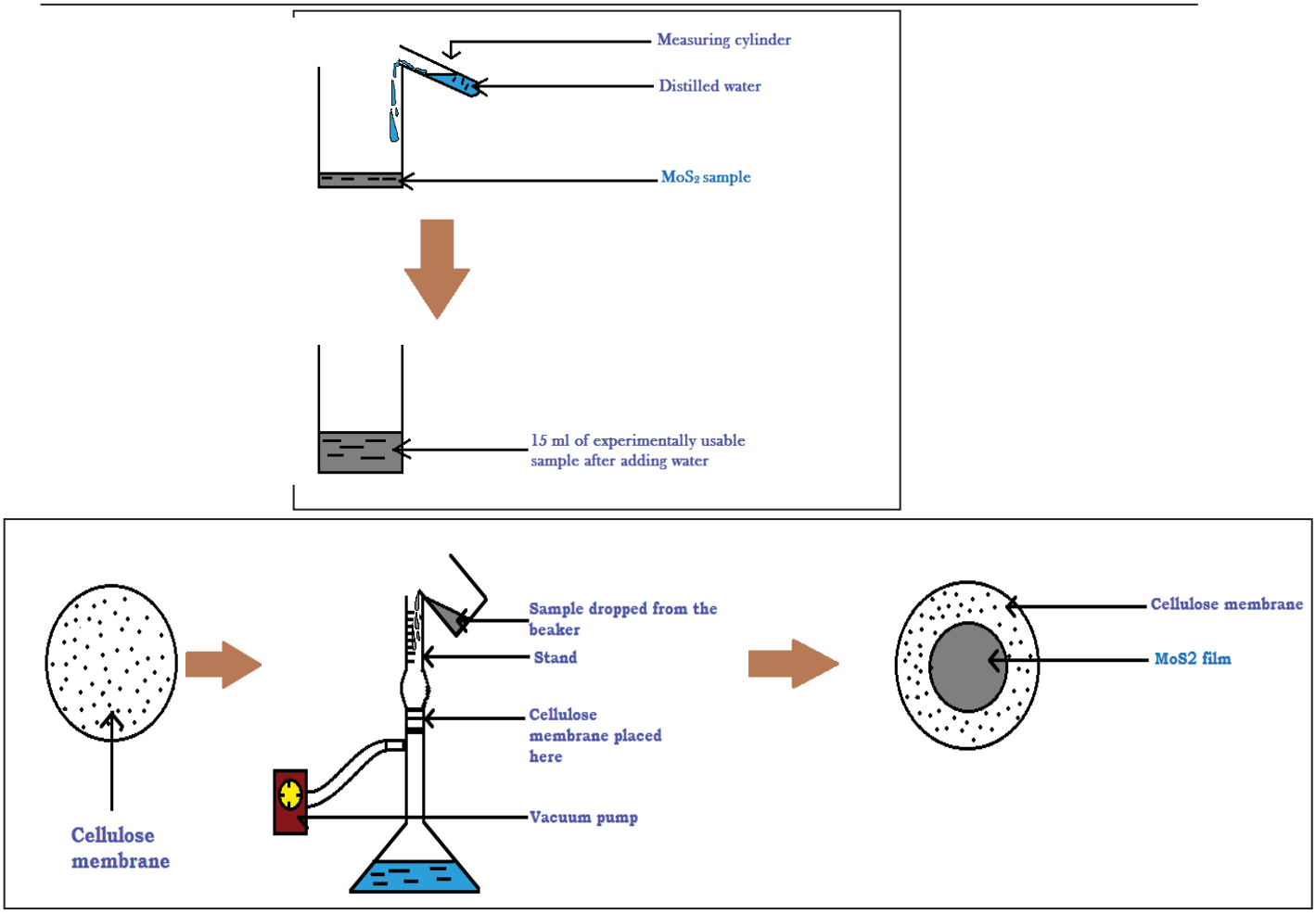

FIG. 4: Pictorial representation of fabricating the thin film of MoS_2

4.6. Preparation of the Gate material

3 gm of PVA is taken in a clean beaker and 30 ml of distilled water is added to it. Now it is stirred well for about 1 hour by keeping it on the stirrer machine and keeping the movable magnetic peddle in it at a temperature of about 80℃. Now, 2 grams of 98% conc. H_2SO_4 is added to it and it is kept on the stirrer for about 6 hours and thus the gate material (PVA+H_2SO_4) is prepared for using in further steps of the experiment.

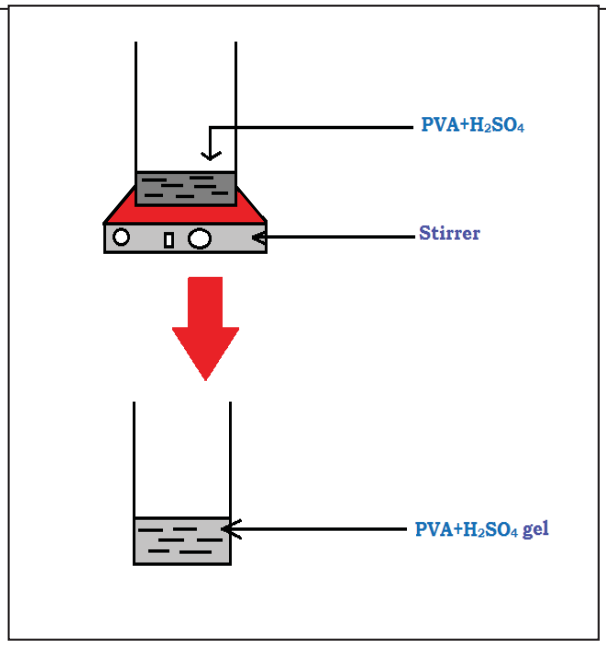

FIG.5: Pictorial representation of preparation of the Gate material

4.7. Fabrication of the device

A channel of width 1 mm is made through the gold-coated PET at the middle of the taken piece by wrapping tissue paper on the end of the forceps and rubbing it on the PET. Now the film of MoS_2 is transferred on the channel of the PET by placing heavy weight on it and the unwanted cellulose is dissolved by holding the PET on the evaporating Acetone. After its almost dissolving, the PET with the channel material is immersed in the acetone bath at room temperature. Thus the channel material is successfully deposited on the channel of the fabricating FET. Now, we have taken two identical pieces of ITO-coated PET half of both of these pieces were pasted with ($PVA+H_2SO_4$) gel with the same thickness and cross sectional area. One piece is kept for the capacitance measurement and copper wire connections were made with it, whereas another piece is taken and pasted well on the channel material of the FET. Now copper wire is connected for source, drain and gate connections. Thus, our device is fabricated.

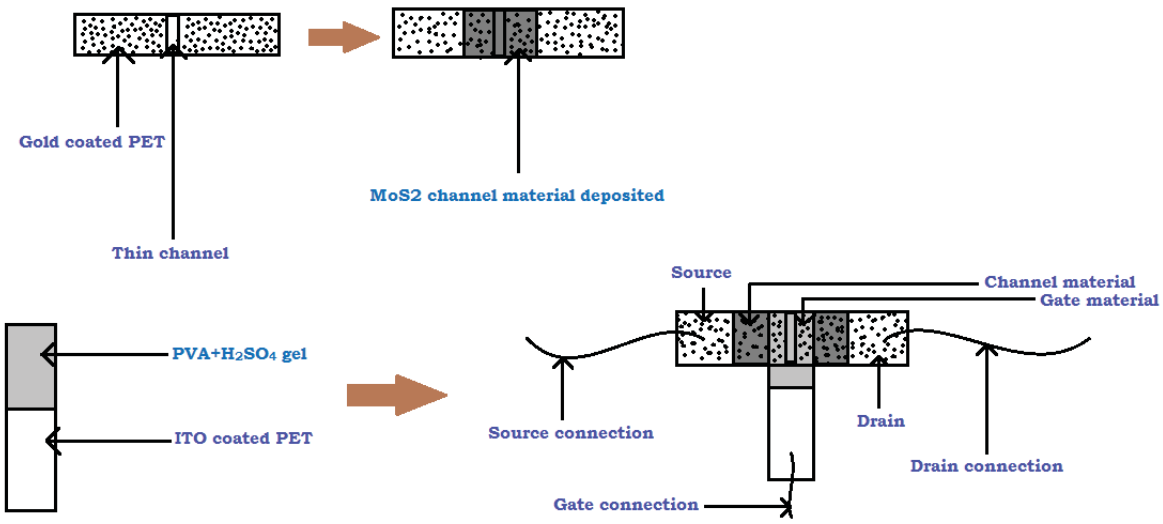

FIG.6: Pictorial representation of fabrication of device

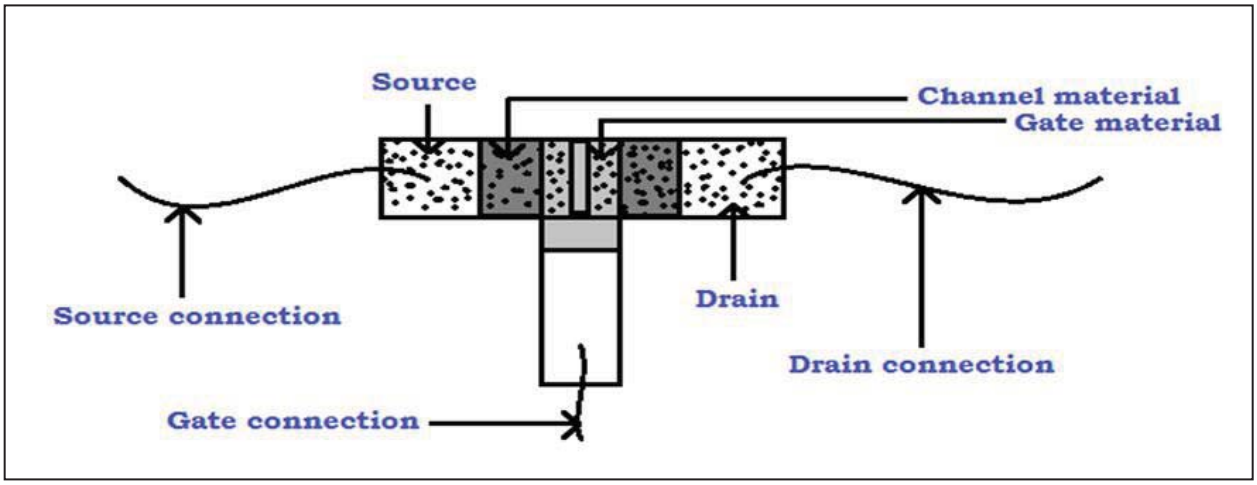

FIG.7: Pictorial representation of our final device

5. Results of the experiment

5.1. Characterization of MoS_2

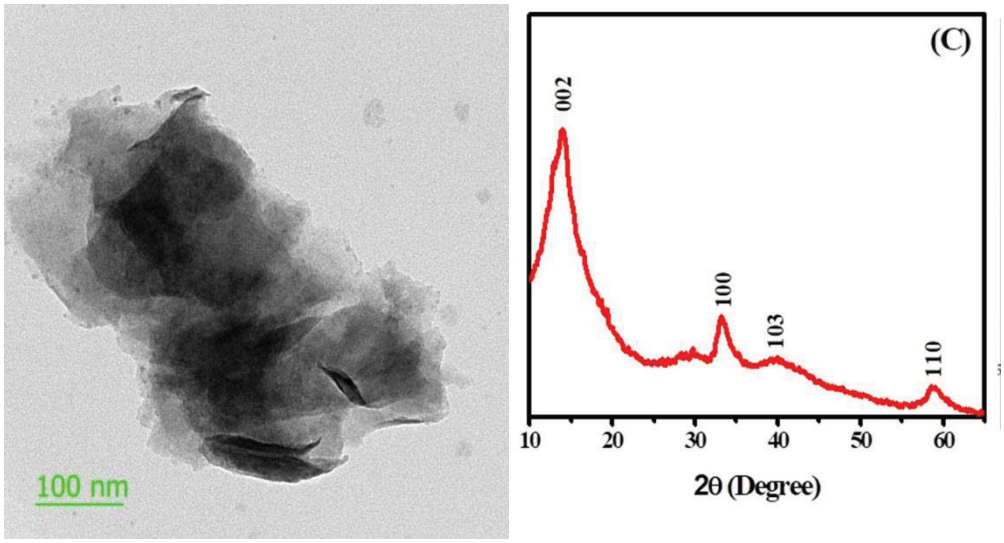

FIG. 8: TEM Image and XRD Image for the Characterisation of MoS_2

So, by analyzing the TEM and XRD data of our prepared MoS_2 and comparing these with the data of several reference review articles, we confirm that our prepared channel material is surely MoS_2.

5.2. Characterization of the EDLT

5.2.1. Drain characteristics

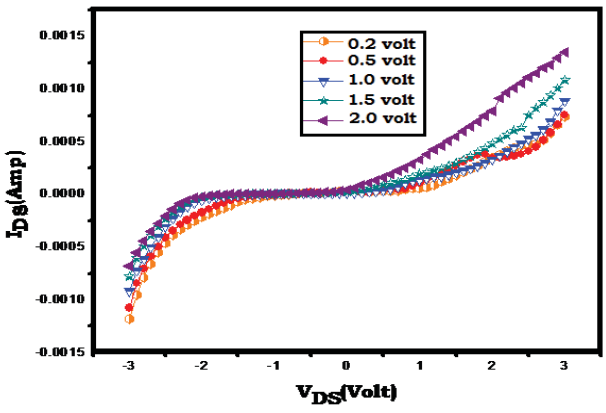

FIG. 9: Drain Characteristics obtained from our experiment

So, here we can see the drain characteristics of the fabricated EDLT, where we can clearly see the presence of the three regions- Ohomic region, saturation region and cut off region. Suppose, that for a given V_{GS} (exceeding the threshold voltage), the drain voltage is made slightly negative with respect to the source. A current flows from the source to the drain through the conducting channel. The channel acts as the resistance so that the drain current I_{DS} is proportional to the drain-to-source voltage V_{DS}. This gives the Ohomic region of the characteristic. The net voltage drop between the gate and the substrate at the drain end of the channel is V_{GS}-V_{DS}, whereas that at the source end is V_{GS}. Consequently the thickness of the channel gradually decreases from the source to the drain. The effect is more prominent with increasing the $|V_{DS}|$. As a result, the channel resistance increases with increases with increasing $|V_{DS}|$, causing the drain characteristic to bend. When V_{DS} attains the value for which V_{GS}-V_{DS}=V_T, the channel thickness at the drain end goes to zero. This is referred to as the pinch-off point. At this point, the drain current saturates at the value of $I_{D,sat}$, the corresponding value of V_{DS} being denoted by $V_{D,sat}$. As $|V_{DS}|$ increases further, the pinch-off point moves towards the source, but the drain current remains almost the same. Thus the saturation region of the drain characteristics is attained. Note that, in the saturation region, I_{DS} slightly increases with V_{DS}. This is the manifestation of the so-called channel-length modulation.

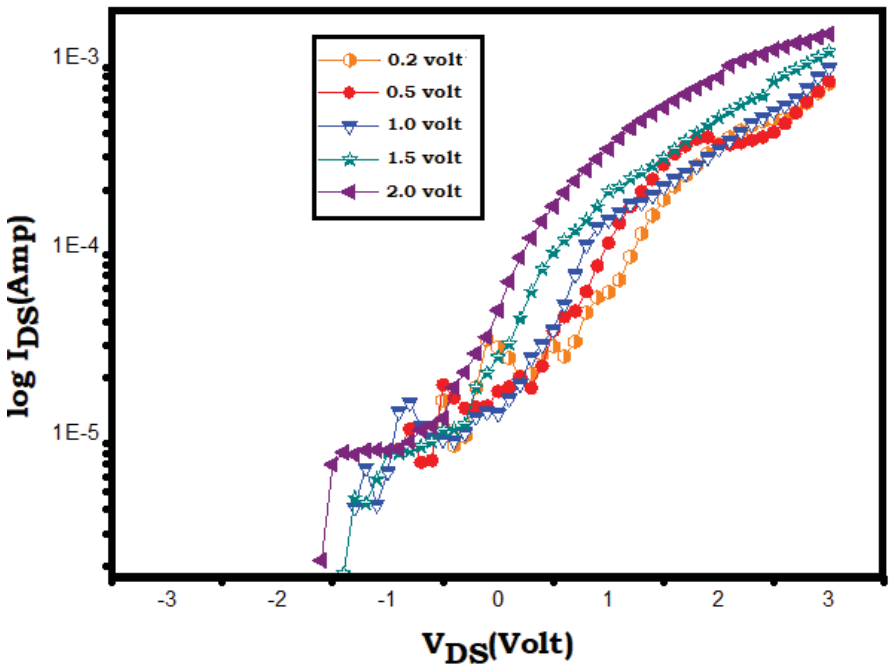

FIG.10: Drain characteristics in Logarithmic Scale

This is the same drain characteristic where the current has been plotted in the logarithmic scale so that we can show the sub threshold increase of the drain current per unit increase of the drain-to-source voltage and this also helps to calculate the sub threshold swing.

5.2.2. Transfer characteristics

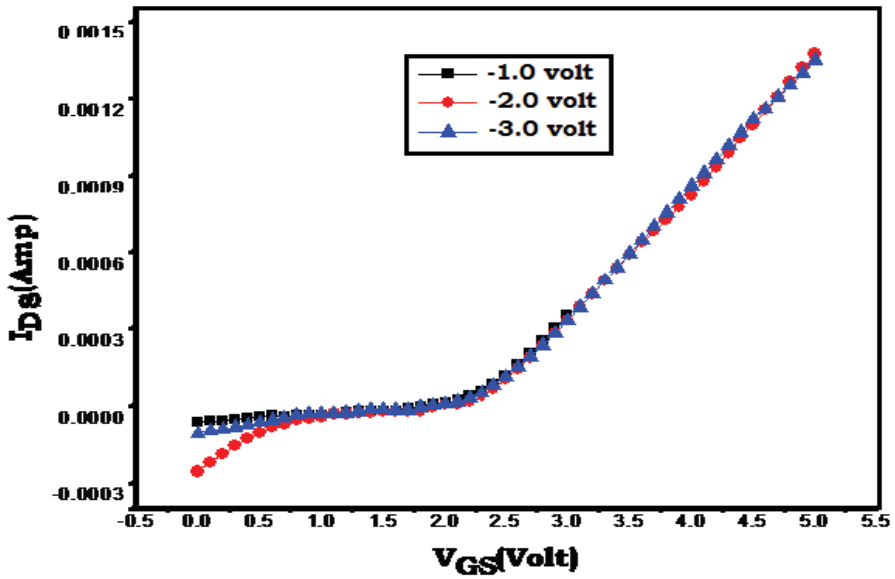

FIG. 11: Transfer Characteristics obtained from our experiment.

The transfer characteristic of the n-channel enhancement type MOSFET is shown in the previous figure. The curve depicts the variation of the drain current with the gate-to-source voltage for a given value of V_{DS}. The transfer characteristic shows that for $V_{GS} \geq 0$, the drain current I_D is very small (typically a few nA). When the V_{GS} is negative, $|I_D|$ rises slowly at first and then rapidly with increasing $|V_{GS}|$.

5.2.3. Values of the parameters (as per the raw data in Ref. 8 and 9)

(i) **Capacitance: 242 µF/cm^2**
(ii) **Field-effect mobility: 60.9 cm^{2}V^{-1}s^{-1}**
(iii) **Transconductance: 477 µS/µm**
(iv) **Sub-threshold swing: 270mV/decade**
(v) **On/off ratio: 100**

6. Future aspects

In future, the investigation of the characteristics and their modification will be continuously interesting, exciting, innovating and highly rewarding. Firstly, Development of flexible devices with outstanding performance and low power operation. Secondly, high density charge accumulation opens a door to understand superconductivity, ferromagnetism, metal insulator transition. Thirdly, the development of solid

state electrolyte for full solid EDLT is of great importance since it couples nanoionics with semiconductor providing high carrier density and excellent compatibility with a wide range of electronic devices owing to its all solid state configuration and many more.

7. Conclusion

The present project represents an attempt of development of the Electric Double Layer Transistor, its working principles, characterization and the electrolyte/semiconductor materials. As expected we have been able to fabricate such device which have larger capacitance, high on/off ratio, lower operational voltage , high transconductance and field-effect mobility which are the key features of a well-behaved EDLT all of whose actions are controlled by the formation of the EDL.

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